VERIFICATION OF A TRANSLATION

I, the translator Dr. Walter Kufner, hereby declare:

My name and post office address are as stated below.

I am knowledgeable in the English language and in the language in which the below identified application was filed, and that I believe the English translation of PCT/DE 03/04015 (WO 2004/050546) filed on December 05, 2003, is a true and complete translation.

All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Full Name of Translator: Dr. Walter Kufner

Walter Kufner

Post Office Address: Stiftsbogen 21
D-81375 München
Germany

PRODUCTION OF MICROMECHANICAL SYSTEMS (MEMS) USING HIGH TEMPERATURE SILICON FUSION BONDING OF WAFERS

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The invention relates to a method for manufacturing MEMS devices, in which the sensor and the electronics for processing the sensor signal are monolithically integrated.

MEMS devices have been manufactured for years on the basis of silicon technologies. Initially, sensor elements have been denoted as MEMS devices, which are composed of a micromechanical portion and a microelectronic portion. The production methods may be divided into two categories according to their micromechanical configuration. On the one hand, a silicon wafer is processed in its total vertical dimension, i.e., it is processed into its depth direction to manufacture structures for the detection of mechanical entities, such as pressure and acceleration (bulk micromachining technologies). On the other hand, such structures are only created at the surface of the silicon wafer (surface micromachining technologies).

The method according to the present invention represents a combination of both types of technologies.

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While initially the sensors for the detection of mechanical parameters and the signal processing electronics (for instance, digital integrated circuits) have been provided as separate entities, the advance in technology calls for the monolithic integration of both components. The integration of micromechanical sensors and electronic circuits in a single chip is demanding with respect to the manufacturing technology, since the manufacturing processes for the sensors are frequently not compatible with the highly integrated CMOS technologies having feature sizes of $\leq 1\mu$. A compromise with respect to achievable performance characteristics (sensitivity, precision, measurement range), integration (feature sizes), reliability and manufacturing cost is necessary.

The specific methodology known for the part of the micromechanical sensors of MEMS devices comprises the patterning of a cavity body, frequently a cavity wafer, by well-established semiconductor process steps, such as oxidation, photolithography, and wet chemical etch processes. In this way, recesses or

depressions are etched into the silicon, which are formed into cavities by covering the same in a later manufacturing stage, wherein the silicon membrane or any other sensor elements that are moveable upon mechanical stress are located above the cavities. After the patterning of the cavity body, it is non-separably bonded to a top cap wafer by means of a wafer bond technique with that side that has formed therein the recesses, so that cavities are formed around the recesses. Thereafter, the wafer stack formed in this manner is processed by silicon grinding and polishing processes, as are well-established in semiconductor processing, thereby significantly thinning the top cap wafer.

DE-A 199 27 970 and DE-A 199 27 971 disclose an intermediate layer deposited on one of the two semiconductor wafers for the formation of cavities. Recesses (depressions) are then formed in the intermediate layer. By means of the intermediate layer, the semiconductor wafer is bonded to a second semiconductor wafer. Thereafter, one of the two semiconductor wafers is thinned to a thickness corresponding to the thickness of the membrane, thereby forming a membrane above the cavity. Since in these instances, the electronic structure is formed in the homogeneously doped wafer material, and since the wafers are connected by means of an intermediate layer formed on one of the semiconductor wafers, apparently the process does not represent a high temperature fusion bond process. Moreover, since the formation of pressure sensors is described, it may be assumed that CMOS specific methods for high integration densities, high values for reliability and production yield, may not be advantageously used. Any defects that may be present in the homogeneous wafer material (Czochralski silicon) may prevent, for instance, the formation of gate oxides having a high quality.

On the other hand, from US-A 5 295 395, it is known in the context of the description of the formation of membrane pressure sensors to use a first semiconductor wafer having an epitaxial layer of inverse doping, by means of which the semiconductor wafer is connected to a second semiconductor wafer by fusion bonding, with a subsequent thinning of the first semiconductor wafer down to the epitaxial layer in such a manner that the membrane is formed by the epitaxial layer. Any hint with respect to a subsequent formation of any signal processing electronic circuitry on the surface of the epitaxial layer is not given. Rather, one may learn from the patent document that after the wafer bonding, no further high temperature step is appropriate, since a fill material is required in the recesses to avoid the deformation of wafer portions of the cap wafer above the recesses during the wafer bond process, wherein the fill material is removed in a later stage.

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In the known publications, there is no hint that the electronic part of the sensors and the signal processing electronics in the form of highly integrated circuitries may be monolithically integrally formed on the basis of the same manufacturing technique.

It is the object of the present invention to increase the sensitivity and the reliability, as well as to decrease the production costs and application costs, of MEMS devices having integrated evaluation electronics. Moreover, an improvement of the production method should be accomplished, so that the sensor-specific portion and the portion of the evaluation electronics of the MEMS device, which is based on CMOS technology, may be manufactured monolithically in a common technology.

This object is solved by the process steps described in claims 1 or 10. Further embodiments of the present invention are described in the dependent claims. The result of the method of the sensor is described in claim 20.

The requirements for the application of a CMOS technology may be fulfilled by providing the specifications of the wafer material of the cap wafer and, in particular, that of the epitaxial layer (dopant, sheet resistance, defect structure) formed on the wafer, wherein the epitaxial layer may specifically have the thickness of the desired membrane, as well as by using high temperature fusion bonding techniques for bonding two semiconductor wafers.

It is within the scope of the present invention that electronic structures may be incorporated into the epitaxial layer of the cap wafer even prior to the wafer bonding process (claim 2), wherein the electronic structures are configured in such a way that they may not significantly be altered by the subsequent high temperature treatment, or the electronic structure may be completed thereby, thus contributing to a densification of the electronic structures or/and contributing to a performance improvement.

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The present invention will be explained and completed on the basis of exemplary embodiments, wherein it should be appreciated that the following description is to be considered as relating to the preferred embodiments of the invention.

Figure 1 is an example of a wafer composite formed by a bulk wafer 2 and an EPI-wafer 1, which are connected by means of a high temperature silicon fusion bonding technique so as to form a wafer composite.

Figure 2 is an example of an absolute pressure sensor using the wafer composite of figure 1.

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Figure 1 shows the bonding of two semiconductor wafers, in the present case, silicon wafers, which are not configured in the same way. They serve the purpose for manufacturing microelectromechanical sensors, wherein the sensors and the signal processing electronics are monolithically integrally formed.

The first wafer 2 is configured as a silicon wafer. The wafer has formed therein a cavity 2a. Also, a plurality of cavities may be provided, wherein for illustrative purposes, a single cavity is illustrated in a magnified manner as a part of a larger wafer. The EPI-wafer carries a substrate formed from silicon and an epitaxal layer, which is denoted as 3. These two wafers 1 and 2 are firmly connected by high temperature fusion bonding via the epitaxial layer 3, i.e., its surface. The recess or cavity 2a is covered and forms a closed cavity.

The wafer composite consisting of both wafers is shown in figure 2 in a further advanced manufacturing stage. The wafer composite has been thinned or reduced from the second wafer 1 down to the epitaxial layer 3. The residual 3a (residual thickness) of the remaining epitaxial layer 3 may be seen from Figure 2 and covers the cavity 2a, thereby forming a cavity 2a (closed or sealed cavity).

The thinning or material reduction is performed to a thickness that corresponds to a thickness of the membrane so as to pick up measurement signals by mechanical deformation of this membrane. The thickness of the remaining membrane 3a corresponds to the micromechanical portion of a sensor 5, which in figure 2 is schematically illustrated as a pressure sensor. The pressure sensors 5 are located above the cavity 2a (i.e., they are registered with respect to the cavity). The thinning may be performed to obtain any other different thickness corresponding to a thickness of any other portion of the semiconductor wafer responding to a mechanical stress, wherein such a portion is not shown.

Subsequently, a polishing step is performed, which is not explicitly shown.

After the polishing process, an electronic sensor structure 4 registered with respect to the cavity is formed on the polished surface in a common process along with one or more analogous and/or one or more digital circuitries by means of an appropriate technology process, in the example shown, a CMOS technology, in order to form the entire SOS wafer 6, which may be considered as a wafer stack.

The sensors 5 are located in the remaining EPI-layer 3a. The circuit elements 4 are located on the remaining EPI-layer and exhibit normal electrical characteristics.

The method results in a reliable overall process having a high yield, which is appropriate for mass production.

The incorporation of structures of electronic circuitries in the epitaxial layer may also be performed prior to the bonding process of the wafers (prior to the bonding) according to figure 1 (not explicitly illustrated).

The EPI-layer 3 may then have incorporated therein structures of the electronic circuitries on that side that faces the cavity 2a for forming the closed cavity after the connection (also not explicitly shown). The electronic structures on the side facing the cavity 2a may, at least after the bonding of the wafers, extend to the polished side (i.e., the surface) and, thus, may, for instance, form electrically conductive channels, which are not explicitly shown.

On the side facing the cavity 2a shall mean that the corresponding electronic structures are formed at least partially in the layer, i.e., in the membrane 3a or at least extend thereto.

The side facing the cavity 2a has, due to said electronic structures, at least one sensor which is not shown, and which is appropriate for the analysis of a medium located adjacent to a membrane 3a in the cavity 2a.

The general methodology, which is referred to with respect to the formation of the electronic sensor structures 4, may not be explicitly described, since these processes are generally known as CMOS technology methods.

A method is described for forming a microelectromechanical system (MEMS), which comprises the monolithical integration of the sensor and the sensor signal processing electronics on the basis of CMOS technologies. By bonding of a semiconductor wafer

(2) having a recess with a wafer having formed thereon an epitaxial layer by means of a high temperature fusion bonding technique via the epitaxial layer (3) so as to form a double wafer, and by a subsequent reduction of the double wafer followed by a polishing process, until the epitaxial layer is exposed, thereby creating a membrane (3a), the prerequisites are given so as to realize the electronic portion (4) of the sensor (5) and the signal processing electronics by means of CMOS technology methods.

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